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EXAMINER	
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ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/527,098	BEUKER, ROB ANNE	
	Examiner	Art Unit	
	TIZE MA	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7 and 9-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,4-5,7,9-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 8/25/2009, with respect to claim rejections under 35 U.S.C. 103(a), have been fully considered but they are not persuasive.

2. Regarding claim 1, the applicant argues that, Hashimoto in view of Badger fails to teach "storing a full table of line pointers for different sequences of video data to be displayed in the memory" and that "a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means" (emphasis added by applicant), as recited in amended claim 1. Specifically, Hashimoto is silent on storing a full table of addresses of the data in the memory array (24) and then downloading a block of the full table of addresses stored in the memory array (24) into the address generators (28a), (28b). Badger fails to teach storing a full table of addresses of the data in the source memory (202) and then downloading a block of the full table of addresses stored in the memory array (24) into the X_Counter and the Y_Counter.

3. The examiner respectfully disagrees. Although Hashimoto did not explicitly state "storing a full table of line pointers in the memory", the equivalent action and result are disclosed in column 5, lines 50-57. In this paragraph, it is stated that "Thus, arbitration and control circuit 30 passes an address generated by address generator 28a to memory array 24 so that data may be written into memory array 24, but a delay may occur due to refresh operations or read accesses of memory array 24. Accordingly, arbitration and control circuit 30 may additionally contain storage devices so that

addresses generated by address generators 28a-28b are not lost when immediate access to memory array 24 is blocked." From this paragraph, one can see that (1) arbitration and control circuit 30 may contain storage devices, which is memory and used for storing addresses; (2) the addresses, including line pointers, are temporarily stored during passing; (3) all addresses are stored, being not lost. In other words, all addresses, including line pointers, are stored in memory. That is basically equivalent to "storing a full table of line pointers in the memory". Therefore the combination of Hashimoto and Badger renders claim 1 obvious to one of ordinary skill in the art at the time of the invention. Claim 1 remains rejected.

4. Similar rationale applies to independent claims 2 and 9. Claims 2 and 9, as well as the dependent claims of claims 1, 2, and 9 also remain rejected.

5. The newly added claims 14-21 are also rejected, since they claim basically various obvious variations of a block, for example, part or half of a line as a block (claims 14-17), or two or more lines as a block (18-21). By definition, a line pointer relates to the line. In the same time, it also relates to any part of the line, or the next line (increment by 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 4-5, 7, 9-10, 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al (US. 5,587,962), and in view of Badger (US. 5,973,664).

8. Regarding claim 1, Hashimoto et al teaches a method of operating a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) , wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer (address sequencers 40a and 40b in Fig. 2), each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line (address generators 28a and 28b in Fig. 2) , the method comprising:

storing a full table of line pointers for different sequences of video data to be displayed in the memory (column 5, lines 50-57, all addresses, including line pointers, are stored in memory, without being lost) ; and

operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from line pointers in address table register means with the output of a pixel counter, and in a second mode wherein line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means (Fig. 3 and column 4, lines 8-11. Two modes of operations, the random access mode and the serial mode. The random access mode is equivalent to the first mode in the instant claim, and the serial mode is equivalent to the second mode).

9. However, Hashimoto et al does not teach a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder.

10. Badger, in the same field of endeavor, teaches a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder (Fig. 8, and column 8, lines 17-39: The image data is a block of lines. The memory address is generated from combining Y_counter and X_counter, associated with the line pointer and pixel counter. The steps 806 and 810 involve additions, which means that a adder, or its equivalence, is present). Displayed image on the screen is often in a 2D rectangular area, which is in a form of block. Using the line counter and pixel counter to form the memory address associates the physical location of the pixel on the image with the memory address. Using a block of line pointers and forming the memory address from line counter and pixel counter are both intuitive method to organize the display data in the memory.

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method as shown in Hashimoto et al by using a block of line pointers and forming the memory address from line counter and pixel counter as shown in Badger for organizing the display data in the memory in an intuitive manner.

12. Regarding claim 2, Hashimoto et al teaches a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) comprising :

a memory for video data to be displayed (memory 24 in Fig. 2) and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for line pointers from said table of line pointers (address sequencers 40a and 40b in Fig. 2); and

means for successively updating the address table register means with subsequent line pointers from the full table of line pointers that is contained in the memory (column 4, lines 8-18, Serial access mode; column 5, lines 50-57, all addresses, including line pointers, are stored in memory, without being lost.)

a pixel counter (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2. As seen in column 6, lines 59-62, although Hashimoto does not directly count pixels, the memory address generated has a direct relation with the location of the pixel, by presetting the beginning address. The size of a pixel is known, usually 4 bits.), the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data (Fig. 3 and column 4, lines 8-11. The random access mode); and

switching means, by which alternately memory addresses for video data are generated in a first mode in the address sequencer, and in a second mode the address

table register is updated with a next block of line pointers from the full table of line pointers that is contained in the memory (column 4, lines 8-18. Serial access mode and random access mode).

13. However, Hashimoto et al does not teach address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder.

14. Badger, in the same field of endeavor, teaches a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder (Fig. 8, and column 8, lines 17-39: The image data is a block of lines. The memory address is generated from combining Y_counter and X_counter, associated with the line pointer and pixel counter. The steps 806 and 810 involve additions, which means that a adder, or its equivalence, is present). Displayed image on the screen is often in a 2D rectangular area, which is in a form of block. Using the line counter and pixel counter to form the memory address associates the physical location of the pixel on the image with the memory address. Using a block of line pointers and forming the memory address from line counter and pixel counter are both intuitive method to organize the display data in the memory.

15. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device as shown in Hashimoto et al by using address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means

using an adder for organizing the display data in the memory in an intuitive manner, as shown in Badger.

16. Regarding claim 4, Hashimoto et al teaches that the memory comprises a full table of line pointers for different sequences of video data to be displayed (column 5, lines 50-52. Writing addresses generated by the address generator into memory).

17. Claim 5 is rejected based on the same reason as to claim 2 since the driving circuit for display system is always connected to a display system if it is operational.

18. Claim 7 is rejected based on the same reason as to claim 2 since they are the software implementation which is necessary to make the circuit in claim 2 operational.

19. Regarding claim 9, Hashimoto et al teaches a driving circuit for a display system comprising:

a memory (Fig. 2, 24) for video data to be displayed and coupled thereto an address sequence for controlling the sequence of writing and/or reading the video data in said memory (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2.)

means for successively updating the address table register means with subsequent line pointers from the full table of line pointers that is contained in the memory (column 4, lines 8-18, serial access mode; column 5, lines 50-57, all addresses, including line pointers, are stored in memory, without being lost); and

a pixel counter, the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2. As seen in column 6, lines 59-62, although Hashimoto does not directly count pixels, the memory

address generated has a direct relation with the location of the pixel, by presetting the beginning address. The size of a pixel is known, usually 4 bits.)

20. However, Hashimoto et al does not teach address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means using an adder.

21. Badger, in the same field of endeavor, teaches a block of line pointers, and generating addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder (Fig. 8, and column 8, lines 17-39: The image data is a block of lines. The memory address is generated from combining Y_counter and X_counter, associated with the line pointer and pixel counter. The steps 806 and 810 involve additions, which means that a adder, or its equivalence, is present). Displayed image on the screen is often in a 2D rectangular area, which is in a form of block. Using the line counter and pixel counter to form the memory address associates the physical location of the pixel on the image with the memory address. Using a block of line pointers and forming the memory address from line counter and pixel counter are both intuitive method to organize the display data in the memory.

22. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device as shown in Hashimoto et al by using address table register means for a block of line pointers and combination with the consecutive line pointers that are read out by a line counter from the address table register means

using an adder for organizing the display data in the memory in an intuitive manner, as shown in Badger.

23. Claim 10 is rejected based on the same reason as to claim 5 since they are the software implementation which is necessary to make the circuit in claim 5 operational.

24. Regarding claims 14 and 16, although Hashimoto et al and Badger do not explicitly teaches wherein a line pointer relates to a part of a picture line, and wherein the pixel counter counts pixels of the part of the picture line, Hashimoto et al and Badger teaches line pointer and pixel counter (Hashimoto et al: column 6, lines 59-67, memory address associated with row and column. Badger: column 7, lines 40-60, mem_pointer with X_increment and Y_increment). By definition, a line pointer relates to the line. In the same time, it also relates to a part of the line.

25. Regarding claims 15 and 17, although Hashimoto et al and Badger do not explicitly teaches wherein a line pointer relates to a half of a picture line, and wherein the pixel counter counts pixels of the half of the picture line, Hashimoto et al and Badger teaches line pointer and pixel counter (Hashimoto et al: column 6, lines 59-67, memory address associated with row and column. Badger: column 7, lines 40-60, mem_pointer with X_increment and Y_increment). By definition, a line pointer relates to the line. In the same time, it also relates to a half of the line.

26. Regarding claims 18 and 20, although Hashimoto et al and Badger do not explicitly teaches wherein a line pointer relates to more than one picture line, and wherein the pixel counter counts pixels of the more than one picture line, Hashimoto et al and Badger teaches line pointer and pixel counter (Hashimoto et al: column 6, lines

59-67, memory address associated with row and column. Badger: column 7, lines 40-60, mem_pointer with X_increment and Y_increment). By definition, a line pointer relates to the line. In the same time, it also relates to next line of the current line, i.e., more than one picture line.

27. Regarding claims 19 and 21, although Hashimoto et al and Badger do not explicitly teaches wherein a line pointer relates to two picture lines, and wherein the pixel counter counts pixels of the two picture lines, Hashimoto et al and Badger teaches line pointer and pixel counter (Hashimoto et al: column 6, lines 59-67, memory address associated with row and column. Badger: column 7, lines 40-60, mem_pointer with X_increment and Y_increment). By definition, a line pointer relates to the line. In the same time, it also relates to the current line and next line, i.e., two picture lines.

28. . Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al, and in view of Badger, as applied to claims 1, 2, and 9 above, and further in view of Jaspers (US. 6,819,326 B2).

29. Regarding claims 11-13, the combination of Hashimoto et al and Badger remains as applied to claims 1, 2, and 9 above, respectively. However, the combination does not explicitly show wherein each block of line pointers is limited to thirty two line pointers, or wherein the number of line pointers in the address table register means is limited to thirty two.

30. Jaspers, also in the same field of endeavor, teaches a block of line pointers is limited to thirty two line pointers (Fig. 2, and column 7, lines 15-22: logical size of memory device keeping the pixels from 32 video lines. Such a logical device is

equivalent to a block of 32 lines. The memory addresses or pointers to the block of lines would be a block of line pointers with 32 line pointers.) This is a convenient choice based on the capacity of the memory device. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method or device as shown in the combination of Hashimoto et al and Badger so that a block of line pointers is limited to thirty two line pointers and the number of line pointers in the address table register means is limited to thirty two as shown in Jaspers based on the capacity of the memory device.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIZE MA whose telephone number is (571)270-3709. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao M. Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628